WHAT IS CLAIMED IS:

1. A phase lock loop (PLL) circuit comprising:

a memory to store a control voltage; and

a processor to load a control voltage, which corresponds to a changed channel, from the memory when a system channel is changed, and to provide the control voltage to a Voltage Control Oscillator (VCO).

2. The PLL circuit of claim 1, wherein the control voltage of the memory is provided to the VCO as an initial value of the control voltage.

3. The PLL circuit of claim 1, wherein once the control voltage of the memory is provided to the VCO, the processor cuts off a path between the memory and the VCO.

4. The PLL circuit of claim 1, wherein the control voltage is stored when a system including a PLL is initialized.

5. The PLL circuit of claim 1, further comprising a signal converter to convert a control voltage to a digital signal and transmit the digital signal to the memory.

6. The PLL circuit of claim 1, further comprising a signal converter to convert control voltage information of the memory to an analog signal and transmit the analog signal to the VCO.

7. The PLL circuit of claim 6, wherein once the analog signal is transmitted to the VCO, the signal converter is disabled.

8. A method for synchronizing a phase of a frequency in a PLL circuit comprising:

storing a control voltage in a memory;

loading the control voltage, which corresponds to a changed channel, from the memory to a VCO; and

setting the control voltage as an initial control voltage.

9. The method of claim 8, further comprising performing a phase lock looping.

10. The method of claim 8, wherein the control voltage is loaded to the VCO when a system channel is changed.

11. The method of claim 8, wherein the control voltage is stored when a system including the PLL is initialized.

12. The method of claim 8, wherein storing the control voltage comprises:

obtaining the control voltage by performing a phase lock looping;

converting the control voltage to a digital signal; and

storing the converted control voltage in the memory.

13. The method of claim 12, wherein storing the control voltage is repeatedly performed until control voltages for every channel of a system are obtained.

14. The method of claim 8, further comprising converting the loaded control voltage information to an analog signal.

15. A phase lock loop (PLL) circuit comprising:

a voltage controlled oscillator (VCO) to output a signal based on a voltage of an input signal;

a memory device to store a control voltage; and

a processor to load the control voltage from the memory device to the VCO.

16. The PLL circuit of claim 15, wherein the processor loads the control voltage from the memory device to the VCO when a system channel is changed.

17. The PLL circuit of claim 16, wherein the control voltage corresponds to a changed channel.

18. The PLL circuit of claim 15, further comprising a signal converter to convert signals from analog to digital and from digital to analog.

19. The PLL circuit of claim 15, wherein the control voltage is used as an initial value of a control voltage of the VCO.

20. The PLL circuit of claim 15, further comprising a frequency generator, a phase detector, a loop filter and first and second frequency dividers.